

MULTIMEDIA



UNIVERSITY

STUDENT ID NO

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MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2018/2019

EEE3196 – INTEGRATED VLSI SYSTEMS
(EE)

11 MARCH 2019
2.30 p.m – 4.30 p.m
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This examination paper consists of 7 pages with 4 questions only.
2. Attempt **ALL FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is given.
3. Please print all your answers in the Answer Booklet provided.

Formulas:

Ideal diode equation: $I_D = I_S(e^{\frac{V_D}{\phi_T}} - 1)$

$$V_T = V_{TO} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

saturation:

$$I_D = \frac{k'_n W}{2L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

linear:

$$I_D = k'_n \frac{W}{L} \left((V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

unified model:

$$I_D = k'_n \frac{W}{L} \left((V_{GS} - V_T) V_{DSAT} - \frac{V_{DSAT}^2}{2} \right) (1 + \lambda V_{DS})$$

$$t_P = \frac{C_L \frac{V_{SWING}}{2}}{I_{AVG}}$$

$$t_P = 0.69 R_{eq} C_L$$

$$P_{dyn} = C_L V_{DD}^2 f$$

Question 1

(a) A resistive-load inverter circuit is given as shown in Figure Q1. Given $V_{DD} = 5\text{ V}$, $k_n' = 30 \mu\text{A/V}^2$, $V_{T0} = 1\text{ V}$, $R_L = 100\text{ k}\Omega$ and $W/L = 3$. Calculate the following critical voltages:

- (i) High output voltage (V_{OH}) [1 mark]
- (ii) Low output voltage (V_{OL}) [8 marks]
- (iii) Noise margins (NM_H and NM_L) for the circuit if given $V_{IL} = 1\text{ V}$ and $V_{IH} = 2\text{ V}$. [4 marks]

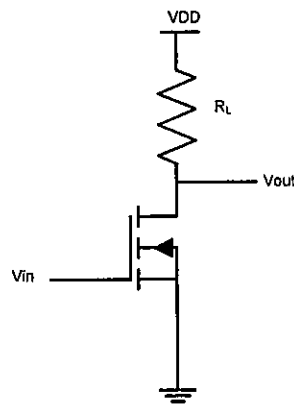


Figure Q1

(b) Given a CMOS inverter with the following parameters:

$k_n' = 50 \mu\text{A/V}^2$, $k_p' = -20 \mu\text{A/V}^2$, $V_{Tn} = |V_{Tp}| = 0.8\text{ V}$, $V_{DD} = 3\text{ V}$, $V_{GS} = 2.5\text{ V}$, $(W/L)_n = 1$, $(W/L)_p = 3$ and $C_L = 30\text{ pF}$.

- (i) Using the average current (I_{avg}) method, find the high-to-low propagation delay (t_{PHL}). [8 marks]
- (ii) Using the average on-resistance (R_{on}) method, find the high-to-low propagation delay (t_{PHL}). [4 marks]

Continued...

Question 2

- (a) Consider a Metal-2 wire with a length of $140\ \mu\text{m}$ and a width of $70\ \mu\text{m}$. Assume a sheet resistance value of $70\ \text{m}\Omega/\text{square}$ and the typical interwire capacitance values are:

$$\text{Area capacitance} = 15.5\ \text{aF}/\mu\text{m}^2$$

$$\text{Fringing capacitance} = 40\ \text{aF}/\mu\text{m}$$

- (i) Calculate the total lumped resistance with this wire.
- (ii) Calculate the total capacitance associated with this wire.
- (iii) Figure Q2 below shows the cross-section of interwire capacitance. Describe ONE of the impacts that can be caused by interwire capacitance.
- (iv) From part (iii), propose TWO methods to reduce the impact caused by the interwire capacitance.

[2+6+2+ 4 marks]

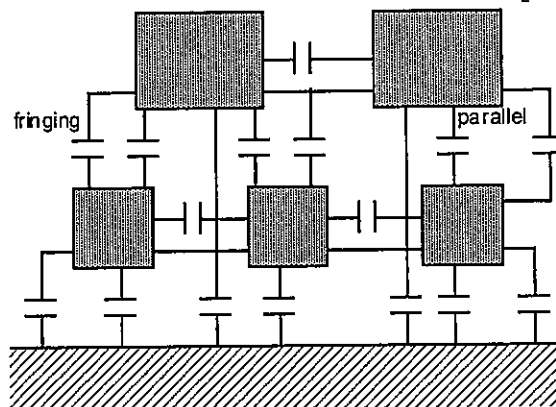


Figure Q2

- (b) Electromigration is a growing concern in on-chip interconnects and it can cause the increased of wire resistance in a circuit, which may result in circuit performance failure.

- (i) Describe the electromigration mechanism.
- (ii) Recommend ONE method to reduce the electromigration phenomenon.

[5+2 marks]

- (c) In electronics manufacturing, integrated circuit (IC) packaging plays an important role in components' operation and performance. Elaborate TWO of the requirements needed for a good IC packaging.

[4 marks]

Continued...

Question 3

- (a) Refer to Figure Q3 below.
- Derive the function, Y for the static CMOS circuit.
 - Modify and re-sketch the circuit in Figure Q3 to the dynamic logic.
 - Based on the modified design in part (ii), describe the operation of the circuit (involving the clock operation).
 - Dynamic designs are known to have some issues and one of the issues is due to charge leakage. Elaborate on the charge leakage issue.
 - Based on part (iv), propose a solution to the charge leakage issue.

[2+4+6+2+2 marks]

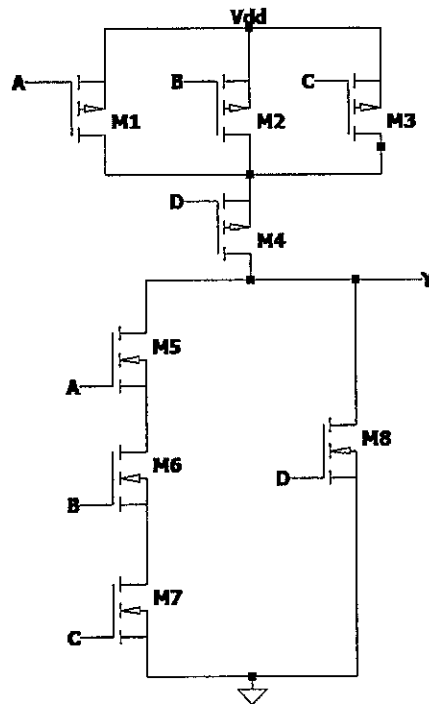


Figure Q3

- (b) Latch and register are static sequential logic circuits.
- Describe the race problem that exists in latch, by giving an example.
 - Propose a solution to reduce or avoid the race problem.

[6+3 marks]

Continued...

Question 4

(a) Given a 8-bit ripple carry adder (RCA) with different delays as listed below:

$$t_{\text{carry}0 \rightarrow 1} = 220\text{ps}, t_{\text{carry}1 \rightarrow 0} = 250\text{ps},$$

$$t_{\text{sum}0 \rightarrow 1} = 320\text{ps}, t_{\text{sum}1 \rightarrow 0} = 350\text{ps}.$$

(i) Find the worst case delay t_{adder} .

(ii) Give an example of input value that will trigger this worst case delay.

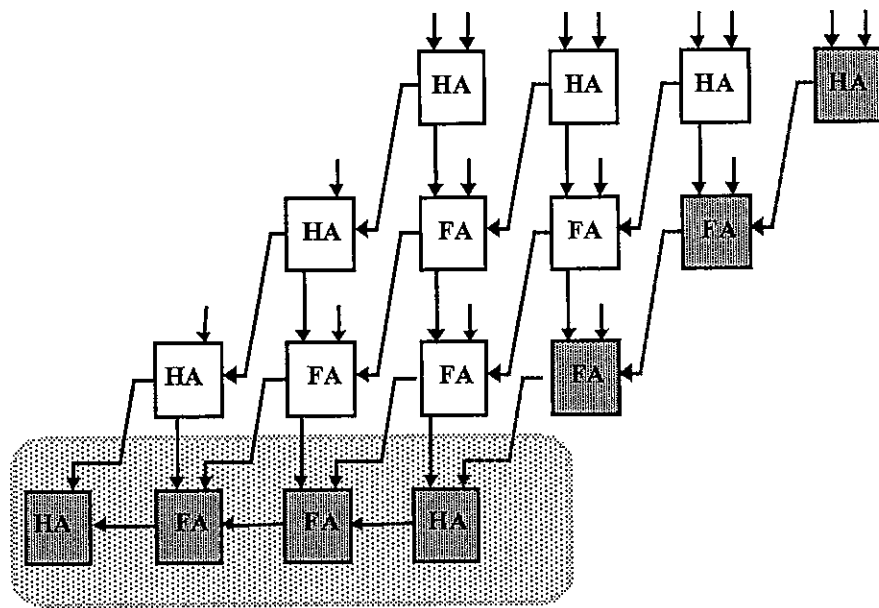
[3+2 marks]

(b) Figure Q4(a) shows a Carry-Save Multiplier circuit which is designed using multiple half adders (HA) and full adders (FA).

(i) Describe the operation of this multiplier especially on the output carry bits and vector merging adder.

(ii) Elaborate on the advantage of this multiplier.

[6+4 marks]



Vector Merging Adder

Figure Q4(a)

Continued...

- (c) Figure Q4(b) shows the performance of different Random Access Memory (RAM) corresponding to the technology node (nm). Thyristor RAM (T-RAM) is another type of DRAM computer memory invented and developed in 2009, combining the strengths of the DRAM and SRAM: high density and high speed.

Comment on the graph. The abbreviation for these memories are:

SRAM=Static RAM, T-DRAM=Thyristor DRAM, SOI=Silicon On Insulator,

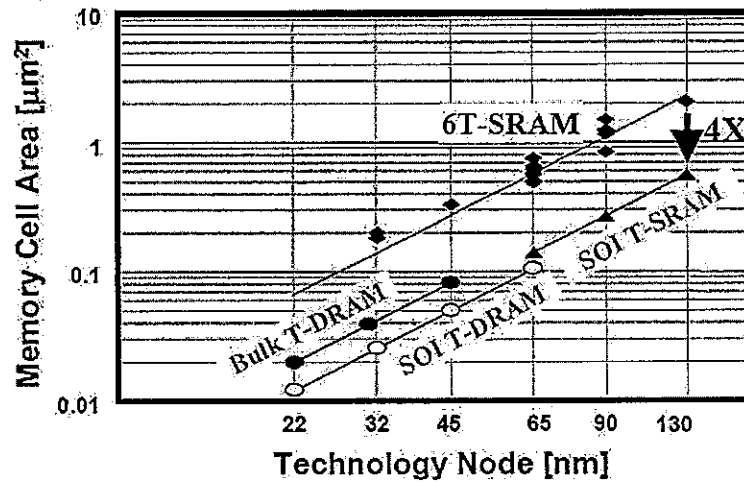


Figure Q4(b)

[4 marks]

- (d) Describe the difference between 1-T DRAM cell and 3-T DRAM cell.

[6 marks]

End of Paper